CIRCUIT AND METHOD FOR CONTROLLING A CLOCK SYNCHRONIZING CIRCUIT FOR LOW POWER REFRESH OPERATION

ABSTRACT OF THE DISCLOSURE

A method and apparatus is provided for idling a clock synchronizing circuit during at least a portion of time during execution of a refresh operation in a memory device. In a memory device receiving an external clock signal, a method and apparatus for executing a refresh operation is provided that includes initiating at least one refresh operation in the memory device, and ceasing generation of an internal clock signal timed with respect to the external clock signal for at least a portion of the time in which at least one refresh operation takes to complete.